Please amend claims 1-5, 9, 13, 15, 18, 19, and 23-26.

1. (Amended) A memory cell comprising:

a source;

a substantially vertical channel formed over the source;

a drain formed over the vertical channel; and

a substantially horizontal floating gate formed over at least a portion of the drain, wherein the square feature size of the memory cell is not greater than $2F^2$.

2. (Amended) The memory cell of claim 1, wherein the source comprises a buried layer.

3. (Amended) The memory cell of claim 1, wherein the horizontal floating gate comprises a sub lithographic floating gate.

4. (Amended) The memory cell of claim 1, wherein the horizontal floating gate comprises a sub lithographic floating gate defined by a spacer.

5. (Amended) The memory cell of claim 1, wherein the horizontal floating gate comprises a self aligned floating gate.

6. A memory cell having a square feature size of less than $4F^2$ comprising:

a source;

a substantially vertical channel formed over the source;

a drain formed over the vertical channel;

a substantially horizontal floating gate formed over at least a portion of the drain; and

a substantially vertical select gate formed substantially perpendicular to the horizontal floating gate in a trench, wherein the select gate is adjacent to the vertical channel.

7. The memory cell of claim 6, wherein the memory cell has a minimum feature size corresponding to the horizontal floating gate and the vertical select gate.

8. The memory cell of claim 6 further comprising a select source and a select drain coupled to the select gate, wherein the select source, the select gate and the select drain form a select transistor.

9. (Amended) The memory cell of claim 6, wherein the memory cell has a square feature size not greater than $2F^2$.

10. A memory cell having a square feature size of less than $4.5F^2$ comprising:

a first transistor comprising a source, a drain and a gate; and

a select transistor coupled to the first transistor, comprising a source, a drain and a gate, wherein the gate of the select transistor is formed substantially perpendicular to the gate of the first transistor.

11. The memory cell of claim 10, wherein the drain of the first transistor has an upper surface and a lower surface and the source of the first transistor has an upper surface and a lower surface and the upper surface of the source of the first transistor is located below the lower surface the drain of the first transistor.

12. The memory cell of claim 10, wherein the source and drain of the first transistor are shared as the source and drain of the select transistor.

13. (Amended) A memory device comprising:

a first n-type layer;

a p-type layer formed over the first n-type layer; and

a second n-type layer formed over the p-type layer, wherein the p-type layer forms a substantially vertical channel, wherein the memory device has memory cells having feature size of less than $4F^2$.

14. The memory device of claim 13, wherein the first n-type layer forms a buried source and the second n-type layer forms a drain.

15. (Amended) A memory device having a square feature size of less than $4F^2$ comprising:

a horizontal first n-type layer formed over a substrate;

a p-type layer formed over the first n-type layer;

a horizontal second n-type layer formed over the p-type layer;

a horizontal floating gate formed over the substrate; and

a vertical select gate formed over the substrate, wherein the p-type layer forms a vertical channel, the first n-type layer forms a buried source and the second n-type layer forms a drain.

16. The memory device of claim 15, wherein the vertical select gate is formed substantially perpendicular to the horizontal floating gate.

17. A memory device having a square feature size of less than $4F^2$ comprising:

a buried source formed over a substrate;

a vertical channel formed over the buried source; and

a drain formed over the vertical channel, wherein the vertical channel is formed using epitaxial deposition.

18. (Amended) A memory device having a square feature size of less than $4F^2$ comprising:

a buried source formed over a substrate;

a vertical channel formed over the buried source; and

a drain formed over the vertical channel, wherein the vertical channel is formed using epitaxial deposition.

19. (Amended) A memory device comprising:

a buried source formed over a substrate;

a vertical channel formed over the buried source;

a drain formed over the vertical channel;

a floating gate formed over the substrate; and

a select gate formed perpendicular to the floating gate in a trench formed in the substrate, wherein the memory device has a square feature size of less than $4F^2$

20. A memory device having a square feature size of less than $4F^2$ comprising:

a substrate having at least one semiconductor layer;

a first n-type layer formed over the substrate;

a p-type layer formed over the first n-type layer;

a second n-type layer formed over the p-type layer;

a floating gate formed over the substrate;

a trench formed in the substrate; and

a select gate formed on a sidewall of the trench.

21. A memory device having a square feature size of less than $4F^2$ comprising:

a substrate having at least one semiconductor layer;

a first n-type layer formed over the substrate forming a source;

a p-type layer formed over the first n-type layer forming a vertical channel;

a second n-type layer formed over the p-type layer forming a drain;

a tunnel oxide layer formed over the n-type layer;

a first poly layer formed over at least a portion of the tunnel oxide layer;

trenches formed in the substrate; and

a select gate formed on sidewalls of the trenches.

22. A memory device having a square feature size of less than $4F^2$ comprising:

a substrate having at least one semiconductor layer;

a buried source formed over the substrate;

a vertical channel formed over the buried source;

a drain formed over the vertical channel;

a tunnel oxide layer formed over the drain;

a self aligned floating gate formed over the tunnel oxide layer;

a trench formed in the substrate;

an active trench formed in the substrate; and

a select gate formed along sidewalls of the active trench area.

23. (Amended) A memory device having a square feature size of less than $4F^2$ comprising:

a first n-type layer formed over a substrate;

a p-type layer formed over the n-type layer;

a second n-type layer formed in the p-type layer;

a select trench formed in the substrate;

a vertical select gate formed in the select trench;

digitlines are formed over the second n-type layer;

a self aligned floating gate formed over the n-type layer; and

wordlines formed over the substrate and the digitlines.

24. (Amended) A memory device having a square feature size of less than $4F^2$ comprising:

a first n-type layer formed over a substrate;

a p-type layer formed over the n-type layer;

a second n-type layer formed in the p-type layer;

a select trench formed in the substrate;

a vertical select gate formed in the select trench;

a conductive layer formed over at least a portion of the second n-type layer;

a first spacer formed on the conductive layer;

a tunnel oxide layer formed over at least a portion of the substrate;

a polysilicon layer formed on the tunnel oxide layer; and

an oxide layer formed on the polysilicon layer.

25. (Amended) The memory device of claim 24, wherein the conductive layer comprises a tungsten layer.

26. (Amended) A memory device comprising:

a first n-type layer formed over a substrate forming a source;

a p-type layer formed over the n-type layer;

a second n-type layer formed in the p-type layer forming a drain;

a select trench formed in the substrate;

a select gate formed substantially vertical in the select trench, wherein the memory device has a feature size substantially less than $4.5F^2$.

27. The memory device of claim 26, further comprising a tunnel oxide layer formed over the substrate.

28. The memory device of claim 27, further comprising digitlines and wordlines formed over the substrate.

29. The memory device of claim 28, wherein the wordlines are above the digitlines.

30. The memory device of claim 29, wherein the wordlines comprise a poly-WSi layer.

31. The memory device of claim 30, wherein the digitlines comprise at least one tungsten layer.

32. The memory device of claim 31, wherein the digitlines are above at least a portion of the drain.

33. The memory device of claim 32 further comprising a spacer formed between the digitlines and the wordlines.

34. The memory device of claim 26, wherein the drain is doped with Boron.

35. The memory device of claim 26, wherein the floating gate comprises tunnel oxide, polysilicon and oxide layers.

36. The memory device of claim 26, wherein the floating gate is self aligned.

IN THE ELECTION REQUIREMENT

The Examiner has required us to elect from the following three inventions:

I. Claims 1-36, drawn to a field effect device with gate electrode in groove.

II. Claims 37-67, drawn to a method of forming FET with additional gate electrode.

III. Claim 68, drawn to a compute system with intrasystem connection.

If Group II is chosen, a single disclosed species will need to be elected from the following Species:

I. Claims 37-40, forming select gate in trench;

II. Claims 41-43, covering a periphery of a wafer using an array mask, epitaxial deposition, wherein thickness of layer determines channel length;

III. Claims 44-47, tunnel oxide, nitride, patterning wordlines, forming STI areas, removing the nitride layer, forming oxide nitride oxide;

IV. Claims 48-56, forming first spacers along sidewalls of the active trench; forming a drain in the active trench and forming a wordline over the drain;

V. Claims 61-67, no trench mentioned.

The applicants hereby elect the invention identified by the Examiner as Invention I for initial prosecution and request examination of claims 1-36.